ABSTRACT OF THE DISCLOSURE

A floating point comparator circuit for comparing a plurality of floating point operands includes a plurality of analysis circuits, one for each of the floating point operands, configured to determine a format of each of the floating point operands based upon floating point status information encoded within each of the floating point operands, and a result generator circuit coupled to the analysis circuits, the result generator circuit configured to generate a result signal based on the format determined by each analysis circuit and based on a comparative relationship among the floating point operands. The format of each of the floating point operands may be from a group comprising: not-a-number (NaN), infinity, normalized, denormalized, zero, invalid operation, overflow, underflow, division by zero, exact, and inexact. The result generator circuit may ignore the encoded floating point statuses of the plurality of floating point operands when comparing just the magnitudes of the plurality of floating point operands.